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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,985	09/07/2000	Anthony M. Chiu	00-C-015	2236

30425 7590 08/05/2003

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/656,985	Applicant(s) CHIU, ANTHONY M.
	Examiner Nitin Parekh	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 8-10, 12, 13, 17 and 18* is/are rejected.

7)☒ Claim(s) *5-7,11 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicants petition under 37 C. F. R. § 1. 144 received on 02-11-03 is treated as a request for reconsideration of the restriction requirement mailed on 11-29-01.

In view of applicant's arguments in paper number 9, the restriction requirement has been withdrawn.

Claim Objections

2. Claims 8 and 9 are objected to because of the following informalities:

A. The claim limitations "packaging encapsulating a portion" as recited in claim 8, line 6, should read "the package having an encapsulated portion".

B. The claim limitations "shorter" as recited in claim 9, line 2, should read " shorter in length".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 8, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamawaki et al. (US Pat. 4894707) in view of Kunii et al. (US Pat. 6252252).

Regarding claim 1, Yamawaki et al. disclose a method of forming an image/photo sensor comprising:

- an integrated circuit (IC)/photosensor chip (1 in Fig. 5f) having a portion remaining exposed after packaging/encapsulating, each IC including a linear/two-dimensional array of 200,000-400,000 image/photosensitive sensors/devices (see area 4 in Fig. 1b;of image/photo sensors; Col. 1, lines 15-20 and 50-55) and a plurality of conventional leads (6 in Fig. 5f) adapted for further mounting/soldering, the packaging method further comprising:
- affixing the IC chip/die to a lead frame (Fig. 5c; Col. 2, line 66)
- connecting the IC die/chip to selected portions of the lead frame with bond wires, (Fig. 5d; Col. 2, line 67)and
- encapsulating a portion of the lead frame and the die except for the exposed region where the exposed region of the die remains exposed to the external light, the encapsulating step comprising: mounting the lead frame, die and the bond wires in a mold (21/22 in Fig. 5e; Col. 3, lines 1-10) with a portion of the mold in contact with the exposed region of the IC die to prevent the encapsulating

material from adhering to the exposed region of the IC die (Fig. 5e; Col. 3, line 50)

(Fig. 5f; Fig. 5a-e; Col. 2, line 50- Col. 3, line 50).

Yamawaki et al. fail to specify mounting the ICs containing the photosensors in alignment on a circuit board and soldering at least some of the leads for each IC to the circuit board.

Kunii et al. teach a conventional method of forming a plurality of optical ICs on a leadframe (see IC 23 and 24 on leadframe 21/22 in Fig. 1) and further teach mounting such plurality of optical ICs/devices on other substrates such as printed circuit substrates/boards, metal substrates, TAB, etc. (Col. 11, lines 1-10). Furthermore, Kunii et al. teach using a circuit board including a plurality/array of optical IC devices, the device packages having soldered leads (see leads of the packaged device 50 on the PWB 48 in Fig. 9) where the optical devices/photo sensors are soldered in a line/alignment (Fig. 9/10; Col. 12, line 3-15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the ICs containing the photosensors in alignment on a circuit board and soldering at least some of the leads for each IC to the circuit board as taught by Kunii et al. so that the device inspection, cycle time and repair capability can be improved in Yamawaki et al's method.

Regarding claim 2, Yamawaki et al. and Kunii et al. teach substantially the entire method of forming the image/photo sensor as applied to claim 1 above, wherein Yamawaki et al. teach the step of forming the ICs comprising:

- affixing the IC chip/die to a lead frame (Fig. 5c; Col. 2, line 66)
- connecting the IC die/chip to selected portions of the lead frame with bond wires, (Fig. 5d; Col. 2, line 67), and
- encapsulating a portion of the lead frame and the die except for the exposed region where the exposed region of the die remains exposed to the external light,

Regarding claims 3 and 4, Yamawaki et al. and Kunii et al. teach substantially the entire method of forming the image/photo sensor as applied to claims 1 and 2 above, wherein Yamawaki et al. teach the steps of mounting the lead frame and encapsulating comprising:

- mounting the lead frame, die and the bond wires in a mold (21/22 in Fig. 5e)
- a portion of the mold being in contact with the exposed region of the IC die to prevent the encapsulating material from adhering to the exposed region of the IC die (Fig. 5e; Col. 3, line 50), and
- the mold having a sloped/tapered surface (see 26 in Fig. 5e) adjacent to the portion contacting the exposed region of the IC where the sloped/tapered surface
- forms one surface of the mold cavity receiving the bond wires when the lead frame with the IC die is mounted in the mold (Col. 3, lines 43-50).

Regarding claim 8, Yamawaki et al. disclose an image/photo sensor integrated circuit (IC) package (1/9 in Fig. 5f) comprising:

- a leadframe including a die paddle/frame and a plurality of leads (5 and 6 respectively in Fig. 5a-5f)
- the IC/die (1 in Fig. 5f) being affixed/bonded to the die paddle/frame (Fig. 5c; Col. 2, line 66), each IC including a linear/two-dimensional array of 200,000-400,000 image/photosensitive sensors/devices (see area 4 in Fig. 1b; Col. 1, lines 15-20 and 50-55) linearly/in two-dimension aligned along the length and width in an area on the upper surface of the IC die,
- bond wires connecting the IC die to selected portions of the leadframe (6 and 8 respectively in Fig. 5d-5f), and
- the package having an encapsulated portion of the lead frame, bonding wires and the die except for the exposed region of the IC die containing image/photosensitive sensors/devices (9 in Fig. 5f) where the exposed region of the die remains exposed to the external light through the packaging

(Fig. 5a-5f; Col. 2, line 50- Col. 3, line 50).

Yamawaki et al. fail to teach using the IC package for a linear photosensor array.

Kunii et al. teach mounting a plurality of optical IC devices/photo sensors on substrates such as printed circuit substrates/boards, metal substrates, TAB, etc. (Col. 11, lines 1-10) where a plurality/array of optical IC devices/photo sensors having

respective leads are soldered to a printed circuit board (see soldered leads on the PCB 48 in Fig. 9; Col. 11, line 1- Col. 12, line 15), the optical devices/photo sensors being in a linear alignment/array (see 50 in Fig. 9 and 10; Col. 12, lines 1-15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC package for a linear photosensor array as taught by Kunii et al. so that the device inspection, cycle time and repair capability can be improved in Yamawaki et al's IC package.

Regarding claim 10, Yamawaki et al. and Kunii et al. teach substantially the entire claimed structure as applied to claim 8 above, wherein Yamawaki et al. teach the IC die being affixed to the leadframe using a conventional method of die bonding/adhesive bonding (Col. 1, line 40; Fig. 4c, 5c, etc.).

Regarding claim 12, Yamawaki et al. and Kunii et al. teach substantially the entire claimed structure as applied to claim 8 above, wherein Yamawaki et al. teach the bond wires connecting the IC die to the selected portions of the leadframe (6 and 8 respectively in Fig. 5d-5f).

Regarding claim 13, Yamawaki et al. disclose an image/photo sensor integrated circuit (IC) package (1/9 in Fig. 5f) comprising:

- a leadframe including a die paddle/frame and a plurality of leads (5 and 6 respectively in Fig. 5a-5f)
- the IC/die being affixed/bonded to the die paddle/frame (Fig. 5c; Col. 2, line 66), each IC including a linear/two-dimensional array/plurality of 200,000-400,000 image/photosensitive sensors/devices (see area/surface region 4 in Fig. 1b; Col. 1, lines 15-20 and 50-55) linearly/in two-dimension aligned along the length and width in an area/surface region on the upper surface of the IC die,
- bond wires connecting the IC die to selected portions of the leadframe (6 and 8 respectively in Fig. 5d-5f), and
- the package having an encapsulated portion of the lead frame, bonding wires and the die except for the exposed surface region of the IC die containing image/photosensitive sensors/devices (9 in Fig. 5f) where the exposed region of the die remains exposed to the external/ambient light through the packaging

(Fig. 5a-5f; Col. 2, line 50- Col. 3, line 50).

Yamawaki et al. fail to teach using the IC package being a linear photosensor array comprising:

- a circuit board

- a plurality of ICs being mounted in a line and linearly aligned array along a length of a surface region of the IC die and a plurality of leads adapted for soldering to the circuit board, wherein the surface regions of each packaged IC being in alignment, and
- at least some of the leads for each packaged IC being soldered to the circuit board.

Kunii et al. teach mounting a plurality of optical IC devices/photo sensors on substrates such as printed circuit substrates/boards, metal substrates, TAB, etc. (Col. 11, lines 1-10) where a plurality/array of packaged optical IC devices/photo sensors having respective leads are soldered to a printed circuit board (see soldered leads on the PCB 48 in Fig. 9; Col. 11, line 1- Col. 12, line 15), the optical devices/photo sensors being in a linear alignment/array (see 50 in Fig. 9 and 10; Col. 12, lines 1-15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the linear photosensor array on a circuit board such that the plurality of ICs being mounted in a line and linearly aligned array along a length of a surface region of the IC die where the surface regions of each packaged IC being in alignment and at least some of the leads for each packaged IC being soldered to the circuit board as taught by Kunii et al. so that the device

inspection, throughput, cycle time and repair capability can be improved in Yamawaki et al's IC package.

5. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamawaki et al. (US Pat. 4894707) in view of Hirai (US Pat. 5384286).

Regarding claim 17, Yamawaki et al. disclose a mold (21/22 in Fig. 5e) for packaging ICs comprising:

- a surface against which a leadframe strip is placed (not numerically referenced in Fig. 5E, see a lower surface of an upper mold 21 contacting leads 6 of the leadframe strip 5/6 in Fig. 5e)
- a plurality of cavity regions extending from the surface placed (24 around the leads 6 under the mold surfaces 26 and 27 forming hollow regions in Fig. 5e; Col. 3, lines 43-50), each cavity region receiving IC die (1/3 in Fig. 5a-5e) affixed to the leadframe strip, the die having bonding wires being connected to the leadframe strip when the leadframe strip is placed against the surface,
- each cavity region being formed by:
    - o a first surface contacting a surface region of the IC die (not numerically referenced in Fig. 5E, see a lower horizontal surface of an upper mold 21 contacting the surface region 3 of the die in a hollow section 25 in Fig. 5e)

when the leadframe strip is placed against the surface to prevent an encapsulate material from adhering the surface/surface region of the IC die (see Fig. 5f), and

- a sloped/tapered surface extending from the first surface of the cavity (26 in Fig. 5e) to form an area receiving the bond wires connecting the IC die to the leadframe strip when the leadframe strip is placed against the surface

(Fig. 5e; Fig. 5a-5e; Col. 3, lines 42-62; Col. 1-3).

Yamawaki et al. fail to teach the surface of the leadframe including projecting pins, the pins being received by the tooling holes when the leadframe is placed against the surface.

Hirai teaches a conventional encapsulating apparatus comprising a mold and a leadframe (120 and 20 in Fig. 1 and 2) where the leadframe include projecting/positioning pins (124 in Fig. 1) which are received by the tooling holes (20b in Fig. 1) when the leadframe is placed against the surface (Col. 3, lines 28-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the leadframe including projecting pins where the pins are received by the tooling holes when the leadframe is placed against the surface as taught by Hirai so that the alignment between the leadframe and the mold can be improved in Yamawaki et al's IC package.

Regarding claim 18, Yamawaki et al. and Hirai teach substantially the entire claimed structure as applied to claim 17 above, and further teaches the cavity regions being contiguous and forms a single cavity (Fig. 5e).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamawaki et al. (US Pat. 4894707) and Kunii et al. (US Pat. 6252252) as applied to claim 8 above, and further in view of Alagaratnam et al. (US Pat. 5814881).

Regarding claim 9, Yamawaki et al. and Kunii et al. teach substantially the entire claimed structure as applied to claim 8 above, except the die paddle being smaller in length dimension than the IC die.

Alagaratnam et al. teach using a leadframe package having a die paddle (12 in Fig. 1) with predetermined length/width/peripheral dimensions, the peripheral dimensions of the die paddle being substantially smaller than those of the IC chip (14 in Fig. 1; Col. 3, lines 30-36).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die paddle being smaller in length dimension than the IC die as taught by Alagaratnam et al. so that the encapsulation defects and the device dimensions and weight can be reduced in Kunii et al. and Yamawaki et al's IC package.

Response to Arguments

7. Applicant's arguments filed on 02-11-03 have been fully considered but they are not persuasive.

A. Applicant contends that Kunii et al. do not teach the IC die containing an array of photosensors.

However, as explained above, Yamawaki et al. teach the IC containing the linear/two-dimensional array of image/photo sensors (see region 4 in Fig. 1a-1c; Col. 1, lines 15-20 and 50-55).

B. Applicant contends that none of the references teach mounting the ICs on the leadframes and then on the circuit board with the photosensors being in an alignment and soldering at least some of the leads.

However, as explained above, Yamawaki et al. and Kunii et al. teach mounting the ICs on the leadframes (Fig. 5a-5f and Fig. 9 respectively) and Kunii et al. teach using the PWB substrate where the optical IC device packages are in the alignment and have respective leads being soldered to the PWB (see IC packages 50 on PWB 48 in Fig. 9 and 10).

Allowable Subject Matter

8. Claims 5-7, 11 and 14-16 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The primary reason for an allowance of claims 5-7, 11 and 14-16 is the inclusion of the limitations of steps of forming a linear photosensor array having a plurality pf packaged ICs where the plurality of IC dice are separated approximately by a distance equal to a kerf width such that the IC packages are in contact with each other, the region containing the photosensors being exposed such that the packaging encapsulant does not cover the ends of the IC die and the leads on one side of the IC packages are in floating contact with conductive structures. The prior art references Yamawaki et al. (US Pat. 4894707), Kunii et al. (US Pat. 6252252) and Alagaratnam et al. (US Pat. 5814881) lack the teachings of mounting and soldering the IC dice such that the IC dice are separated approximately by a distance equal to a kerf width while the packaged ICs are in contact with each other having the encapsulant exposing the ends of the IC die packages and the leads on one side of the IC packages being in floating contact with conductive structures on the circuit board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
07-24-03

Tom Thomas

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